HIGHLY ORDERED SEMICONDUCTOR NANOTUBES GROWN ON WAFER-SCALE PATTERNED GRAPHENE LAYERS

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Bottom-up approach for the growth of semiconductor nanostructures on various rigid substrates has been investigated extensively as a promising method for fabricating practical and efficient nanoelectronic and optoelectronic devices [1]. However, the choices of the underlying substrates are limited due to the common lattice mismatch problem between different solids, high-cost issues of single crystals, and poor supply of high-quality materials. Since its discovery in 2004, graphene arises as a powerful solution for an ideal 2D platform for both fundamental and industrial research sectors. We have demonstrated hybrid semiconductor nanostructures using thin graphene layers as an interfacial growth layer deposited on any types of solid substrates [2]. It was shown that high-quality, smooth, and flat ZnO thin films on graphene layers can be grown to yield excellent photoluminescence and enhanced light emitting characteristics. In this talk, we report the growth of highly-ordered 1D semiconductor nanostructures on wafer-scale graphene layers for advanced and high-end applications. It is evident that CVD graphene layer plays a critical role to control the growth of uniform 1D nanomaterials with various aspect ratios without defects over a wide area. The nanoscale physical properties at the interfaces and junctions are investigated by TEM, SEM, and AFM probes. Finally, as promising applications of ZnO nanotubes grown on large-area graphene layers via a standard MOCVD process, flexible light-emitting devices and nanotube-array capacitors will be presented.

Keywords: ZnO nanotubes, CVD graphene, Nanoelectronics

References:


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